Remarks

I. Status of the Claims

In the Office Action, the Examiner indicated that claims 1-16 are pending, and are rejected.

II. General Comments

On page 2 of the Final Office Action, the Examiner clearly explains that Olsen does teach of time multiplexing data transmission on nonfaulty signal conductors. Applicants agree with the Examiner that claims 1-16, as presented earlier are not allowable over Olsen and the combination references cited by the Examiner.

The Examiner also notes on page 3 of the Final Office Action "...that for k=1, 'J/(K-F)' would render the claims to be unclear or indefinite. Applicants believe that claim 1 is not unclear or indefinite, for, in the case that K=1 (i.e., a one signal conductor bus) there can be no faulty signaling conductors. Applicants believe that, e.g., in claim 1, "...over a signaling bus having 'K' signaling conductors, where zero to 'K-1' of the signaling conductors is faulty...", there can be no faulty signaling conductors (F must = 0), and 'J/(K-0)' is clear and definite. Although the Examiner did not object or reject any claims based upon this concern, Applicants respectively request that the Examiner reconsider and withdraw his concern on this item.

The Examiner states on page 2 that "...features upon which applicant relies (i.e., transmit data on every nonfaulty signaling conductor) are not clearly recited in the rejected claim(s)." (Claim 1-12). Applicant respectfully disagrees with the Examiner. In Claim 1, Applicants most clearly state: "...transmitting the 'J' bit block of data over the 'K-F' nonfaulty signaling conductors using 'J/(K-F)' beats, plus an additional beat if a remainder exists." Applicants believe that it is clearly recited that the data is transmitted over the "K-F" nonfaulty signaling conductors.

III. Rejections based on Prior Art – 35 USC §102

On Page 4 of the Office Action, the Examiner rejects Claim 13 under 35 U.S.C. 102(b) as being anticipated by Olsen (US 5,440,538).

As above, Applicants are in agreement with the Examiner regarding Olsen's broad teaching regarding time multiplexing data over nonfaulty signaling conductors. Applicants also agree with the Examiner's "103" rejections of Claims 14-16 over Olsen and Becker, found in paragraph 7, page 9 of the Final Office Action. **Applicants cancel Claims 13-16.**

III. Rejections based on Prior Art – 35 USC §103

On page 4, 5 of the Final Office Action, the Examiner states: "Claims 1-2, 6-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Olsen (US 5,440,538)** and in further view of **Izuno et al. (US 5,717,852)**."

Applicants disagree with the Examiner's arguments on pages 5 and 6, with reference to Olsen's Fig. 2, which has "spare" signaling conductors, wherein Applicants' claim does not have "spare" signaling conductors. Applicants responded to similar arguments in the response dated 8/31/2007.

However... Applicants note that Olsen, in Fig. 12, 13A-13H, and associated specification does teach of time multiplexing data over signaling conductors where no "spare" signaling conductors are required. Claims 1 and 8 clearly need to be amended to distinguish over Olsen, as found in Olsen's Fig. 12, 13A-13H and teachings in Olsen's specification regarding Fig. 12, 13A-13H.

The Examiner properly rejects claim 2 over Olsen and Izuno. Olsen, in Fig. 12, 13A-13H, does store data bits not "sendable" because of faulty signaling conductors. Olsen stores the unsent bits in registers 54a-54g, as shown, e.g., in Fig. 12, rendering Applicants' original Claim 2 unpatentable as well as Claim 1.

Applicants amend Claim 1 to include the limitations of Claims 1, 2, 3, and 4. Claims 3-5 were rejected in paragraph 6, page 7, of the Office Action under Olsen, Izuno, and in further view of Becker et al. (US 2004/0136319A1). Applicants respectfully disagree with the Examiner's rejection of Claims 3-5.

Applicants respectfully submit that, on page 10 of the August 31, 2007 response, a compelling argument was made as to why Becker's shift register is an inappropriate reason to reject Applicant's Claim 3. Applicants acknowledge, however, regarding Applicants' argument (copied below), that Claim 3 did not explicitly include transmitting bits of the shift

register to a nonfaulty conductor. In the present amendment, limitations of Claim 4 are further amended into Claim 1 to correct that deficiency. For the Examiner's convenience, that argument is repeated below (with highlighting added):

The Examiner relies on Becker for a "shift register unit (e.g., items 402-406, fig. 4) for storing data bits".

Applicants respectfully point out that **shift register bits 402-406 are not connected in a manner wherein bits in the shift register can even be driven on a signaling bus**. Rather, Becker's shift register is used by Becker's test control logic 434 to provide data that is compared against data received on Becker's chip from receivers 414, 416, and 418. **No teaching is made, as required in Claim 3, of shifting "at least one bit of the 'F' bits into a first end of a shift register." "F" bits are bits that would have been transmitted in a beat, but were directed to faulty signaling conductors and therefore could not be transmitted on the same beat that data was transmitted over nonfaulty signaling conductors.** Applicants respectfully submit that the fact that Becker "has a shift register" does not make obvious the use of a shift register as claimed in Claim 3 to store bits that would have been transmitted on a particular beat, but for a fault on a signaling conductor.

Applicants believe that Claim 1, as amended, including limitations of Claims 2, 3, and 4, is allowable over Olsen, Izuno, and Becker and respectfully requests the Examiner to reconsider and allow Claim 1, as amended.

Claims 5 and 6 have been amended to depend from Claim 1. Applicants believe that Claim 1, as amended, is allowable, making Claims 5 and 6 allowable by dependency.

Claim 7 depends from Claim 1, which Applicants believe to be allowable. Claim 7 is allowable by dependency if Claim 1 is allowable.

On page 6 of the Final Office Action, the Examiner rejects Claims 8-11 under 35 U.S.C. 103(a) over Olsen and Izuno.

In response, **Applicants amend Claim 8** to narrowly claim the teachings of Applicants' Fig. 3 (and additional details provided in Figs. 4-6). In particular, Applicants' Fig. 3 shows but a single shift register (driving bit register 27). Description of Fig. 3 on pages 11-14 of Applicants' specification describes operation of the apparatus, using a shift register implementation. Although mention is made on page 12 of replications of driving bit register 27, only a single instance of driving bit register is shown and described, providing explicit support for a single faulty signaling conductor. Applicants believe that, while explaining that, by replicating "driving bit register 27", extensions to multiple failing bits would be

readily understood by one of skill in the art, that Claim 8, as amended, is readily allowable. Therefore, Claim 8 is narrowly constructed to support of a single faulty signaling conductor.

As explained earlier, Olsen, Izuno, and Becker singly, or in combination, do not fairly teach, suggest, or motivate, storage (and later transmission) of bits unable to bits unable to be transmitted in a beat because of existence of a faulty signaling conductor in a shift register, let alone use of rotations of the shift register as taught by Applicants. Therefore, Applicants respectfully submit that Claim 8, as amended, is allowable.

Claims 9-12 are cancelled.

IV. Conclusion

In view of the foregoing comments and amendments, Applicant respectfully requests that the application, with Claims 1,5-7, and 8 be passed to issue.

If the Examiner believes that a telephone interview with Applicants' agent would be helpful in speeding prosecution, Applicants' agent would encourage a telephone interview at the number below.

Respectfully submitted,

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